ACADEMIC AFFAIRS OFFICE
INDIAN INSTITUTE OF TECHNOLOGY ROORKEE

No. Acd./ 4232 /IAPC-88 Dated: August 08, 2020

Head, Department of Electronics & Communication Engineering

The IAPC in its 88th meeting held on 30/31.07.2020 under **Item No. 88.2.10** considered the proposed syllabus of Department of ECE to replace an existing course CS-221 (Computer Architecture and Microprocessors) with a new course i.e. ECN-207 (Computer Architecture and Organization).

The IAPC accepted the syllabus of ECN-207 with minor modifications. Duly modified syllabus is attached as **Appendix-A**.

Reeti

Assistant Registrar (Curriculum)

Encl: as above

Copy to (through e mail):-

1. All faculty
2. All Heads of Departments/ Centres
3. Dean, Academic Affairs
4. Associate Dean of Academic Affairs (Curriculum)
5. Channel I/ Academic webpage of iitr.ac.in/ acad portal

INDIAN INSTITUTE OF TECHNOLOGY ROORKEE

NAME OF DEPARTMENT: Electronics and Communication Engineering

1. **Subject Code:** ECN-207 **Course Title:** Computer Architecture and Organization
2. **Contact Hours:** **L:** 3 **T:** 1 **P:** 0
3. **Examination Duration (Hrs.):** **Theory:** 3 **Practical:** 0
4. **Relative Weightage:** **CWS:** 20-35 **PRS:** 0 **MTE:** 20-30 **ETE:** 40-50 **PRE:** 0
5. **Credits:** 4 **6. Semester:** Autumn **7. Subject Area:** PCC
8. **Pre-requisite:** Introductory knowledge of Boolean algebra, digital logic, sequential/memory elements and finite state machines.
9. **Objective:** To learn basics of computer architecture and organization.

10. Details of the Course

Sl. No.	Contents	Contact Hours
1.	Metrics for evaluating application performance, evaluating and summarizing performance, energy management approaches (e.g., DVFS)	4
2.	Floating-point number system (IEEE-754), esp. FP-16, FP-32, FP64 representations. Fixed-point and integer representation.	4
3.	Basics of cache and memory hierarchy, caches in multicore processors, translation lookaside buffer (TLB) for virtual memory. Practical experiments will involve designing cache simulator.	7
4.	A simplified RISC-based processor architecture; Instruction set, instruction types and formats; Instruction execution, instruction cycles, different types of machine cycles and timing diagram. Practical experiments will be conducted using a simulator of this processor.	7
5	Instruction set principles, machine instructions, types of operations and operands, encoding an instruction set, assembly language programming, addressing modes and formats. All these will be for the simplified RISC-based processor discussed above.	7
6	Processor design and pipelining, pipelining hazards, superscalar/pipelined/out-of-order designs	7
7.	Systolic array for matrix multiplication, DRAM architecture	3
8.	I/O organization; I/O techniques: interrupts, polling, DMA; Synchronous vs. asynchronous I/O.	1
9.	Multiprocessing, multithreading and vectorization	2
	Total	**42**

11. Suggested Books:

Sl. No.	Name of Books/ Authors	Year of Publication
1.	Computer Architecture: A quantitative approach (Fifth Edition), by J. L. Hennessy and D. A. Patterson, Morgan Kaufmann.	2012
2.	Computer Organisation and Architecture, by S. R. Sarangi, McGrawHill India.	2014
3.	Recent relevant research papers will be provided by the instructor	-